Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte HIROMI YAMASHITA

Appeal No. 1999-2691
Application No. 08/590,348

ON BRIEF

Before HAIRSTON, KRASS, and BARRY, Administrative Patent Judges.
HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 4 through 7.

The disclosed invention relates to an image signal processing apparatus.

Claims 4 and 7 are illustrative of the claimed invention, and they read as follows:

4. An image signal processing apparatus, comprising:

an image sensor for reading an image and outputting image data representing the read image as an image data signal;

a sample-and-hold circuit for sampling and holding said image data signal for a predetermined output period;

an A/D converter for converting an analog signal outputted by said sample-and-hold circuit corresponding to a held image data signal into a digital signal;

a reference signal generator for generating a reference signal;

a timing generator for generating a read timing signal which is used to read out image data from the image sensor for a predetermined reading period and a hold timing signal which controls hold timing of the sample-and-hold circuit according to said reference signal; and

an A/D conversion timing generator for generating a conversion timing signal according to said reference signal for controlling operation of said A/D converter;

wherein said timing generator changes either said read timing signal or said hold timing signal so that the same data from the starting point of the output of the image data is held, when changing the output period of the image data for image enlargement or reduction processing.

7. An image signal processing apparatus, comprising:

an image sensor for reading an image and outputting image data representing the read image as an image data signal;

a sample-and-hold circuit for sampling and holding said image data signal;

an A/D converter for converting an analog signal outputted by said sample-and-hold circuit corresponding to a held image data signal into a digital signal; and

means for preventing said A/D converter from inputting said analog signal at the same time that said analog signal changes its value.

The references relied on by the examiner are:

Hasegawa et al. (Hasegawa)	4,691,114	Sept. 1, 1987
Hasegawa et al. (Hasegawa)	4,891,690	Jan. 2, 1990
Hirota	5,132,788	July 21, 1992
Higashitsutsumi	5,144,445	Sept. 1, 1992

Claim 7 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Hasegawa '690.

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirota in view of Higashitsutsumi.

Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirota in view of Higashitsutsumi and Hasegawa '114.

Reference is made to the briefs (paper numbers 15 and 17) and the answer (paper number 16) for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will sustain the 35 U.S.C. § 102(b) rejection of claim 7, and we will reverse the 35 U.S.C. § 103(a) rejection of claims 4 through 6.

Turning first as we must to the 35 U.S.C. § 102(b) rejection of claim 7, the examiner indicates (answer, page 4) that Hasegawa '690 discloses (Figure 13) an image sensor 21, a sample-and-hold

circuit 132 and an A/D converter 135 as claimed. According to the examiner (answer, page 4), the "pulse Gen. for A/D 138 can prevent the A/D converter 135 from inputting the analog signals at the same time that the analog signal changes it[s] value, see col. 7 and 8, lines 1-68, Figs. 13-17)." Appellant argues (brief, page 9) that:

> [B]ecause the pulse generators receive the same system clock from frequency generator **f**, the pulses produced by generators 137 and 138 will be in phase, and will have frequencies that are certain multiples of each other. Over time, therefore, there inevitably will occur a point at which the A/D clock pulse is produced at the same time that an analog image signal value is sampled and latched by the sample/hold circuits. Contrary to the assertion in the final Office action, Fig. 15B in fact shows an example of such simultaneous occurrence of signal SMPC (7) and A/D CLK R (17), as well as simultaneous occurrence of SMPY signal (9) and A/D CLK B, G (16). Further, it is emphasized that the timing waveforms of Figs. 15B and 17 represent only a finite sample of the clock pulse trains, which continue to be produced during operation of the apparatus for an extended period of time during image scanning.

In response to appellant's arguments, the examiner directs appellant's attention to "Figs. [sic, Fig.] 15B, signal SMPG (8) and A/D CLK B, G (16) and Fig. 15A" (answer, page 7). According to the examiner, "when the SMPG signal level is High (on) (i.e., the analog signal changes its value), the A/D CLK B, G signal level is Low (off) at that time, therefore, the A/D converter is inherently preventing [sic, prevented] from inputting an analog signal during

its Low signal level where the SMPG signal changes its value (i.e., High) at that time."

We agree with appellant that the noted overlapping times are instances in which Hasegawa does not perform the function of "preventing said A/D converter from inputting said analog signal at the same time that said analog signal changes its value." On the other hand, we agree with the examiner that during the time period when "signal SMPG (8) and A/D CLK B, G (16)" do not overlap, Hasegawa has a "means for preventing said A/D converter from inputting said analog signal at the same time that said analog signal changes its value." Inasmuch as nothing in claim 7 on appeal precludes Hasegawa '690 from having a "means for preventing" the A/D converter from inputting analog signals at a specified time as well as a means for allowing the A/D converter to input analog signals at a specified time, we find that claim 7 reads entirely on the noted limited time period in Hasegawa '690 for "preventing said A/D converter from inputting said analog signal at the same time that said analog signal changes its value." Thus, the 35 U.S.C. § 102(b) rejection of claim 7 is sustained.

Turning next to the 35 U.S.C. § 103(a) rejection of claim 4, appellant and the examiner both agree (brief, pages 10 and 11; answer, page 5) that Hirota does not disclose a timing generator

that "changes either said read timing signal or said hold timing signal so that the same data from the starting point of the output of the image data is held, when changing the output period of the image data for image enlargement or reduction processing." For such a teaching, the examiner turned to Higashitsutsumi. According to the examiner (answer, page 5), "Higashitsutsumi '445 teaches the use of the timing generator (i.e., 111, 112 and 113) for changing the read timing signal so that the same data from the starting point of the output of the image data is held during the image reduction process (see Figs. 7, 8, 10 and 22, col. 6, line 50 - col. 8, lines [sic, line] 68." The examiner is of the opinion (answer, pages 5 and 6) that the combined teachings of the references would "produce a high-quality reproduced picture by using a solid-state image apparatus having a small number of pixels as taught by Higashitsutsumi."

Appellant argues (brief, page 11) that Higashitsutsumi "does not utilize any A/D conversion of CCD image signals, but to the contrary inputs the CCD image signals directly to a display," and is completely irrelevant to the invention set forth in claim 4. We agree with appellant's arguments. Higashitsutsumi is directed to an image pickup apparatus 110, and to the circuitry 111, 112 and 113 (Figure 7) for controlling the operation of the image pickup

apparatus. The control circuitry 111 through 113 in Higashitsutsumi is incapable of performing any of the functions ascribed to it by the examiner (answer, page 5). For these reasons, the 35 U.S.C. § 103(a) rejection of claim 4 is reversed.

The 35 U.S.C. § 103(a) rejection of claims 5 and 6 is reversed because the teachings of Hasegawa '114 do not cure the noted shortcomings in the teachings of Hirota and Higashitsutsumi.

DECISION

The decision of the examiner rejecting claim 7 under 35 U.S.C. § 102(b) is affirmed, and the decision of the examiner rejecting claims 4 through 6 under 35 U.S.C. § 103(a) is reversed. Accordingly, the decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON Administrative Patent Judge	)
ERROL A. KRASS Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)

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APPEAL NO. 1999-2691

APPLICATION NO. 08/590,348

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DECISION: **AIP**

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OB/HD

PALM

ACTS 2

DISK (FOIA)

REPORT

BOOK